CLAIMS

What is claimed is:

1. A data transmission method for microprocessors in a programmable logic controller, which defines two microprocessors as a master microprocessor and a slave microprocessor, which method is characterized in that: the master microprocessor and the slave microprocessor have two corresponding I/O pins for sending and receiving data signals through one pin and sending pulse-wave signals through the other.

2. A data signal used in a data transmission method for microprocessors in a programmable logic controller comprising:

a command code character, which defines the initial value of data;

an initial address character, which follows the command code character and defines the initial address of data;

a data-length character, which follows the initial address character and defines the data length; and

at least one data-conception character, which follows the data length character.

3. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the character comprises eight data bits, one parity bit, and a responding bit.

4. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the first through fourth bits of the command code character determine the transmission rate of data.

5. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the fifth bit of the command code

character is used to confirm the transmission rate.

6. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the sixth through eighth bits of the command code character defines the transmission protocol of data.

7. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 6, wherein a 16-bit read-out mode is selected if the sixth through eighth bits are 000.

8. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 6, wherein an 8-bit read-out mode is selected if the sixth through eighth bits are 011.

9. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 6, wherein a 16-bit write-in mode is selected if the sixth through eighth bits are 101.

10. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 6, wherein a 16-bit write-in mode is selected if the sixth through eighth bits are 110.

11. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the ninth bit of the command code character is a parity bit for sending the same bit as a check of data transmissions.

12. The data signal used in a data transmission method for microprocessors in a programmable logic controller of claim 2, wherein the tenth bit of the command code character is a responding bit for confirming that the data transmission is complete.